ACM/SIGDA FPGA 2008

2nd Annual Pre-Conference Workshop

Designing with Extreme Parallelism

Sunday, Feb 24, 2:00 pm – 5:30pm
Pinos-Alones Room (4th floor)
Workshop Goals

• Welcome ideas on CAD, architecture, and novel mainstream uses of FPGAs

• Plan the course for future FPGA-related research in general

• Create a vision and inspire young researchers with technical ideas, funding avenues, and relevance
Last Year’s Workshop

• Grand Challenges on FPGA Research
• Key findings
  – Jason Cong: Optimality gap in CAD?
  – Kurt Keutzer: Applications-to-hardware bridge
  – Grant Martin: Stop focusing on FPGAs!
  – Vaughn Betz: Compile/design time, power, I/O
  – Steve Trimberger: Timelines, dog food, binary compatible
  – Jonathan Rose: ASIC/FPGA gap, more theory
  – André DeHon: Defects, variation, transients
Designing with Extreme Parallelism

- FPGAs hold millions of gates
  - Not just your grand-daddy’s glue logic anymore…

- FPGAs build large, digital systems
  - Lots of inherent parallelism (it’s hardware!)

- Time-to-system is key advantage of FPGAs
  - Compile time?
  - Design time?
  - Synthesis from high level programming tools?
Designing with Extreme Parallelism

• Custom compute engines
• Orders of magnitude
  – Speedup
  – Lower power

• Parallel language tools?
  – For ASICs
  – For FPGAs
  – For other parallel systems?
Designing with Extreme Parallelism

- Designing Parallel Systems with High-level Languages
  - Overview of Parallel Landscape
  - Catapult C (Mentor Graphics)
  - Mitrion C (Mitrionics)
  - Reconfigurable Toolbox (DSPlogic)
  - CUDA (NVIDIA)
Format and Time Table

**Session 1 (2:00pm)**
- Prof. Tarek El-Ghazawi, *GWU*
- Dr. Andres Takach, *Mentor Graphics*
- Dr. Michael Babst, *DSPlogic*

**Break (3:30pm)**

**Session 2 (4:00pm)**
- Mr. Stefan Möhl, *Mitrionics*
- Dr. David Kirk, *NVIDIA*
- Open Discussion

**End (~5:30pm)**

**FPGA 2008 Registration (6:00pm)**
**FPGA 2008 Reception (7:00pm)**
Prof. Tarek El-Ghazawi

- Dept of ECE, The George Washington University
- Co-Director of NSF CHREC
- Director of Institute of Massively Parallel Applications and Computing Technologies (IMPACT), GWU

- Major developer of Unified Parallel C (UPC)
  - Author of UPC book
- Assoc. Editor IEEE Trans. on Computers
Dr. Andres Takach

- Chief Scientist, Mentor Graphics
- C-based hardware synthesis
- Faculty member at Illinois Institute of Technology 1993 – 1997
- PhD from Princeton in 1993
Michael Babst

- President and Founder of DSPlogic, Inc

- High-Performance Reconfigurable Computing and FPGA-based Digital Signal Processing

- Founding member and Vice President of Eka Systems, a wireless networking startup

- Over 16 years of product development and management experience at General Electric Aerospace, Lockheed Martin, Comsat Laboratories, and Viasat

- Ph.D. from the Pennsylvania State University
Break
Format and Time Table

Session 1 (2:00pm)
• Prof. Tarek El-Ghazawi, GWU
• Dr. Andres Takach, Mentor Graphics
• Dr. Michael Babst, DSPlogic

Break (3:45pm)

Session 2 (4:15pm)
• Mr. Stefan Möhl, Mitrionics
• Dr. David Kirk, NVIDIA
• Open Discussion

End (~5:45pm)

FPGA 2008 Registration (6:00pm)
FPGA 2008 Reception (7:00pm)
Stefan Möhl

- Co-founder of Mitrionics AB in 2001
  - Vice President
  - Chief Scientific Officer
- Researches processor architecture and language design in the context of parallel processing
- Studied Computer Science, Philosophy, Linguistics and Psychology
- Founder of e-commerce startup Shopsense in 1999
David Kirk

- Chief Scientist at NVIDIA since 1997
- Leads NVIDIA’s graphics technology development
- Elected to the National Academy of Engineering (NAE) – 2006
- SIGGRAPH Computer Graphics Achievement Award – 2002
- Chief Scientist, Head of Technology for Crystal Dynamics, 1993 to 1996
- Engineer at Apollo Systems Division (HP), 1989 to 1991
Open Discussion