

Workshop

Designing with Extreme Parallelism

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Modern FPGAs can implement large, custom compute engines that are designed to exploit extreme amounts of parallel computation. Through parallelism, these systems achieve orders of magnitude higher performance than the fastest microprocessors. Building such custom compute engines with existing hardware design languages is too difficult and time-consuming. For this to become mainstream technology, the task of designing such parallel systems must be as simple as possible. Thus, high-level languages are needed which can specify a custom compute engine or be compiled to run on predefined parallel systems. In this workshop, we will examine several approaches for specifying extremely parallel computations in high-level languages. These can be used to build parallel systems in FPGAs, or they can be used to specify parallel computations in other competing architectures. By examining several different approaches, one gains insight into the best approach for solving a given problem. Ideally, this will also inspire new approaches for designing with extreme parallelism.

1. Overview
Prof. Tarek El-Ghazawi, The George Washington University
2. “Synthesis of Technology-Independent Untimed C++”
Dr. Andres Takach, Chief Scientist, Mentor Graphics Corp.
3. “The Mitrion Platform”
Stefan Mohl, CTO, Mitrionics
4. “The Reconfigurable Computing Toolbox”
Dr. Michael Babst, President, DSPlogic
5. “CUDA: Programming Massively Parallel Processors”
Dr. David Kirk, Chief Scientist, NVIDIA
6. “Programming the Cell Broadband Engine”
Dr. Fabrizio Petrini, IBM TJ Watson Research Center

Categories and Subject Descriptors

B.6.1 [Logic Design]: Design Styles – Parallel circuits; D.1.3 [Programming Techniques]: Concurrent Programming – Parallel programming

General Terms

Algorithms, Design, Languages, Performance

Keywords

Custom compute engine, FPGA, hardware description language, high-level electronic design, parallel processing, reconfigurable computing